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D. Remarks

Oath/Declaration

Applicants submit herewith a new declaration for better scan-in quality. It is hoped that these papers are acceptable.

Claim Objections.

Claim 11 has been amended to address the stated objections.

Rejection of Claims 1-3, 5-6, 9, 15-17 Under 35 U.S.C. §102(b) based on *Chang '325* (U.S. Patent No. 5,687,325).

The rejection of claims 1-3, 5-6 and 9 will first be addressed.

The invention of claim 1 is directed to an integrated circuit device that includes a programmable portion comprising a plurality of circuits configurable by a user of the integrated circuit device and at least one communication portion. The communication portion comprises a plurality of data operation circuits, each of which performs a different function on received input data, including at least one circuit block manufactured to perform a predetermined data communication function including converting received first data values into second data values. The at least one circuit includes a block converter circuit that converts an input data word into an output data word having different bit values than the input data word in response to a user selectable operational value, and an operation control store that provides the user selectable operational value from a plurality of operational values to the at least one circuit to control the type of operation performed on the received data. The integrated circuit device also includes a memory circuit for storing configuration information for configuring circuits of the programmable portion.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference. Because the reference *Chang '325* does not show all elements of claim 1, this ground of rejection is traversed.

As emphasized above, Applicants' amended claim 1 recites a "block converter circuit" that "converts an input data word into an output data word having different bit values than the input data word".

FIG. 1 of *Chang '325* does not appear to show any "block converter circuit", as recited in

claim 1. The only circuits apparent in this figure are timing circuits (Event Timers 12, Interrupt Controller 14, System Timers 18, Real-Time Clock 22), a data transfer circuit (DMA Controller 16) and data storage (RAM Cache 24) circuits. None of these circuits is shown or suggested to convert data words as recited in amended claim 1.

Similarly, FIG. 2 of *Chang '325* does appear to show any "block converter circuit" like that of claim 1. FIG. 2 shows a RAM DAC 64, but such a circuit does not convert "an input data word into an output data word having different bit values than the input data word". Instead, such a circuit converts a binary input data value into an analog value for driving a display:

> Within the RAM DAC 64, the color value specified by the CLUT is presented to DACs included in the RAM DAC 64 which convert CLUT data values into analog signals... (*Chang '325*, Col. 6, Lines 53-56).

Accordingly, because the reference is not believed to show or suggest all the limitations of amended claim 1, this ground for rejection is traversed.

The rejection of claims 15-17 will now be addressed.

Amended claim 15 is directed to a semiconductor device that includes a programmable logic device having a communication portion embedded therein. The communication portion includes non-programmable circuits designed to provide a selectable data communication function. The non-programmable circuits comprise a block converter circuit that encodes input data words into output data words and a scrambler circuit that scrambles data values according to a user selectable scrambling polynomial, and an operational control store that provides the user selectable scrambling polynomial value to the scrambler circuit from a plurality of user selectable scrambling polynomial values.

Claim 15 has been amended to include of limitations of dependent claim 18 directed to a scrambling function. Claim 18 was not rejected based in *Chang '325*. Accordingly, this ground for rejection is traversed.

Rejection of Claims 1-3, 6-7, 13-16, and 18-21 Under 35 U.S.C. §102(e) based on *Chang '087* (U.S. Patent No. 6,260,087).

The rejection of claims 1-3, 6-7 and 12-14 will first be addressed.

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As noted above, the invention of amended claim 1 includes at least one circuit that includes a block converter circuit that converts an input data word into an output data word having different bit values than the input data word in response to a user selectable operational value.

Chang '087 shows a serial data I/O 32. However, such a circuit is never described as converting an input data word into an output data word having different bit values. Accordingly, the reference is not believed to show or suggest all the limitations of this claim.

The rejection of claims 15-16 and 18-20 will now be addressed.

Claim 15 has been amended to include of limitations of dependent claim 18 directed to a scrambling function. *Chang '087* is not believed to include any teachings or suggestions related to data scrambling according to a polynomial value. A word search of the reference shows that the terms "polynomial" or "scrambling" are not present in the reference.

Accordingly, the reference is not believed to show or suggest all the limitations of this claim.

The rejection of claim 21 will now be addressed.

Amended claim 21 is directed to a method, comprising the steps of performing predetermined logic functions on a programmable logic portion of an integrated circuit and performing serial data communication functions on a communication portion of the integrated circuit that includes circuit blocks that are not synthesized with programmable logic device configuration data. The serial data communication functions are user selectable between (i) selecting a polynomial value from a number of user selectable polynomial values, and scrambling serial data according to the selected polynomial value, or (ii) encoding serial data having words of a first bit length into serial data having words of a second bit length that is different than the first bit length.

To address this ground of rejection Applicants incorporate by reference herein the comments set forth above for claims 15-16 and 18-20. In particular, the cited reference does not show or suggest all the limitations of the claim.

Rejection of Claim 4 Under 35 U.S.C. §103(a), based on *Chang '325* in view of *Freedman* (U.S. Patent No. 3,851,258).

To the extent that this ground for rejection relies on *Chang '325*, Applicants incorporate by reference herein the comments set forth for amended claim 1. In particular, the reference does not show or suggest particular limitations of Applicants' claim 1, thus a prima facie case of obviousness has not been established.

Rejection of Claims 8 and 22-23 Under 35 U.S.C. §103(a), based on *Chang '087* in view of *Tzukerman et al.* (U.S. Patent No. 6,724,829).

The rejection of claim 8 will first be addressed.

To the extent that this ground for rejection relies on *Chang '325*, Applicants incorporate by reference herein the comments set forth for amended claim 1. In particular, the reference does not show or suggest particular limitations of Applicants' claim 1, thus a prima facie case of obviousness has not been established.

The rejection of claims 22 and 23 will now be addressed.

Claim 21 has been amended to include the limitations of claims 22 and 23. As noted above, amended claim 21 includes "serial data communication functions are user selectable between (i) selecting a polynomial value from a number of user selectable polynomial values, and scrambling serial data according to the selected polynomial value".

Applicants' have previously shown in the comments for claim 21 above that *Chang '087* is silent as to polynomial based scrambling. The other reference relied upon, *Tzukerman et al.*, shows the scrambling of data. However, such scrambling is not based on a polynomial selected by a user from a plurality of such polynomials, but rather a sequence of pseudorandom polynomials:

> A data scrambler 306... scrambles the coded data using a bit sequence provided by a pseudorandom number (PN) generator 305. The PN generator 305... produces a pseudorandom bit sequence that repeats periodically. (*Tzukerman et al.*, Col. 4, Lines 19-25).

For this reason, the cited combination of references not believed to show or suggest all the limitations of amended claim 21, and a prima facie case of obviousness has not been established.

Rejection of Claim 10 Under 35 U.S.C. §103(a), based on *Chang '325* in view of *Tzukerman et al.*

To the extent that this ground for rejection relies on *Chang '325*, Applicants incorporate by reference herein the comments set forth for amended claim 1. In particular, the reference does not show or suggest particular limitations of Applicants' claim 1, thus a prima facie case of obviousness has not been established.

Rejection of Claim 11 Under 35 U.S.C. §103(a), based on *Chang '325* in view of *Devanagundy et al.* (U.S. Patent No. 6,148,384).

To the extent that this ground for rejection relies on *Chang '325*, Applicants incorporate by reference herein the comments set forth for amended claim 1. In particular, the reference does not show or suggest particular limitations of Applicants' claim 1, thus a prima facie case of obviousness has not been established.

Rejection of Claim 12 Under 35 U.S.C. §103(a), based on *Chang '325* in view of *Beal et al.* (U.S. Patent No. 6,791,353).

To the extent that this ground for rejection relies on *Chang '325*, Applicants incorporate by reference herein the comments set forth for amended claim 1. In particular, the reference does not show or suggest particular limitations of Applicants' claim 1, thus a prima facie case of obviousness has not been established.

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Claims 1, 4, 8, 10-15, 19 and 21 have been amended. Claims 3, 6-7, 9, 18, 20 and 22-23 have been cancelled.

The present claims 1-2, 4-5, 8, 10-17, 19 and 21 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

7/7/05

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